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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/933,166	08/21/2001	Yuji Sano	122.1466	6450

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STAAS & HALSEY LLP
700 11TH STREET, NW
SUITE 500
WASHINGTON, DC 20001

EXAMINER
LEE, WILSON

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/933,166	Applicant(s) SANO ET AL.	
	Examiner Wilson Lee	Art Unit 2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) *41-62* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29,32,33 and 35-40* is/are rejected.

7)☒ Claim(s) *30,31 and 34* is/are objected to.

8)☒ Claim(s) *41-62* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Remarks

Claims 41-62 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected inventions, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Claim Rejections – 35 U.S.C. 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4-9, 12-18, 21-25, 28, 29, 32, 33, 35, 38-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Katayama et al. (6,556,177).

Regarding Claim 1, Katayama discloses a capacitive load (4) driving circuit comprising:

- a driving device (5) connecting a driving power supply source (9) to an output terminal (5a) connectable to a capacitive load (4); and
- a power distributing circuit (12 and 13, or 10 and 11) connected between the driving power supply source (9) and the driving device (5) (See Figure 3).

Regarding Claim 4, Katayama discloses that the power distributing circuit is inherently a constant-current source since it renders unchanged current directly from the power source (9).

Regarding Claim 5, Katayama discloses that the driving power supply source (9) outputs a plurality of different voltage levels in a selective manner controlled by the power transistors (10 and 11) such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 6, Katayama discloses that the power distributing circuit includes a plurality of power distributing units (power transistors 10 and 11), one for each of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 7, Katayama discloses that each of the power distributing units (10 and 11) has a function as a switch for selecting one of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 8, Katayama discloses that the driving device (5) is a device whose input withstand voltage is inherently higher than an output voltage since Katayama discloses the driving device (5) has high voltage endurance (See Col. 4, lines 10-11) so that it can withstand high voltage and the output voltage is lowered in order to prevent blowing up the voltage sensitive loads.

Regarding Claim 9, Katayama discloses a capacitive load driving circuit comprising: a driving device comprising a reference potential (terminals +, -) of the power source (9) to an output terminal (5a); and a power distributing circuit (12 and 13) between the reference potential point (terminals +, -) and the driving device (5) (See Figure 3).

Regarding Claim 12, Katayama discloses that the power distributing circuit is inherently a constant-current source since it renders unchanged current directly from the power source (9).

Regarding Claim 13, Katayama discloses that the driving power supply source (9) outputs a plurality of different voltage levels in a selective manner controlled by the power transistors (10 and 11) such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 14, Katayama discloses that the power distributing circuit includes a plurality of power distributing units (power transistors 10 and 11), one for each of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 15, Katayama discloses that each of the power distributing units (10 and 11) has a function as a switch for selecting one of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 16, Katayama discloses that the driving device (5) is a device whose input withstand voltage is inherently higher than an output voltage since Katayama discloses the driving device (5) has high voltage endurance (See Col. 4, lines 10-11) so that it can withstand high voltage and the output voltage is lowered in order to prevent blowing up the voltage sensitive loads.

Regarding Claim 17, Katayama discloses a capacitive load driving circuit comprising:

- a plurality of driving devices (6) driving a plurality of capacitive loads (4) and formed in integrated-circuit form (See abstract); and

- a power distributing circuit (15, or 12 & 13, or 10 & 11) connecting each of the plurality of driving devices (6) to a driving power supply source (9) or to a reference potential point (terminals +, -) (See Figures 1, 3 or 4).

Regarding Claim 18, Katayama discloses that a diode (shown in Figure 5A) inserted between each of the capacitive loads (4) and a corresponding one driving devices (6) (See Figure 6).

Regarding Claim 21, Katayama discloses that the power distributing circuit (12 & 13) is inherently a constant-current source since it renders unchanged current directly from the power source (9).

Regarding Claim 22, Katayama discloses that the driving power supply source (9) outputs a plurality of different voltage levels in a selective manner controlled by the power transistors (10 and 11) such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 23, Katayama discloses that the power distributing circuit includes a plurality of power distributing units (power transistors 10 and 11), one for each of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 24, Katayama discloses that each of the power distributing units (10 and 11) has a function as a switch for selecting one of the plurality of different voltage levels such as voltage dividing (See Col. 10, lines 34-36).

Regarding Claim 25, Katayama discloses that the driving device (5) is a device whose input withstand voltage is inherently higher than an output voltage since Katayama discloses the driving device (5) has high voltage endurance (See Col. 4, lines

10-11) so that it can withstand high voltage and the output voltage is lowered in order to prevent blowing up the voltage sensitive loads.

Regarding Claim 28, Katayama discloses that a series connection (5b) of each of the power distributing circuit (15) and a switch device (10) is provided between each of the driving devices (6) and the driving power supply source (9) (See Figures 1 and 4).

Regarding Claim 29, Katayama discloses that the capacitive load driving circuit is constructed as a driving module (5) containing a plurality of driving integrated circuits (6) for driving the capacitive loads (4) (See Figure 1).

Regarding Claim 32, Katayama discloses a switch device (10 or 11) inserted between the power distributing circuit (15) and the driving power supply source (9) and the switching being caused to conduct after the driving devices (7) have been switched into a conducting state (See Figure 5B. Switch device is in conductive state when driving device (7) is also in conductive state).

Regarding Claim 33, Katayama discloses a capacitive load driving circuit including a configuration in which a driving power supply source (9) is connected to an output terminal (5a) via a driving device (5), wherein the driving power supply source (9) outputs a plurality of different voltage levels in a selective manner by voltage dividing (See Figure 1 and Col. 10, lines 34-36).

Regarding Claim 35, Katayama discloses a capacitive load driving circuit for driving a capacitive load (4), connected to an output terminal (5a), by a driving device (5), comprising a resistive impedance (12 and 13) inserted in series to the output terminal (5a) (See Figure 3).

Regarding Claim 38, Katayama discloses that a driving power supply source (9) connected to the output terminal (5a) via the driving device (5); and a power distributing circuit (12 and 13) inserted between the driving power supply source (9) and the driving device (5) (See Figure 3).

Regarding Claim 39, Katayama discloses that a reference potential point (terminals +, -) of the power source (9) connected to the output terminal (5a) via the driving device (5); and a power distributing circuit (12 and 13) inserted between the reference potential point (+, -) and the driving device (5).

Regarding Claim 40, Katayama discloses that a plurality of driving devices (6) for driving a plurality of capacitive loads (4), formed in integrated-circuit form (See abstract), wherein each of the driving devices is connected to a driving power supply source (9) or a reference potential point (terminals +, -) via a power distributing circuit (12 and 13) (See Figure 3).

Claims 1, 9, 17, 26, 27, 33, 35, 38-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyazaki (6,501,467).

Regarding Claim 1, Miyazaki discloses a capacitive load driving circuit comprising:

- a driving device (A1-A5) connecting a driving power supply source (VI1) to an output terminal (V1-V5) connectable to a capacitive load (C1); and
- a power distributing circuit (R1-R5) connected between the driving power supply source (VI1) and the driving device (A1-A5) (See Figure 3).

Regarding Claim 9, Miyazaki discloses a capacitive load driving circuit comprising:

- a driving device (A1-A5) connecting a reference potential point (VI2-VI5) to an output terminal (upper terminal of C1, or V1-V5);
- a power distributing circuit (R1-R5) inserted between the reference potential point (VI2-VI5) and the driving device (A1-A5) (See Figure 2).

Regarding Claim 17, Miyazaki discloses a capacitive load driving circuit comprising:

- a plurality of driving devices (A1-A5) driving a plurality of capacitive loads (C1-C5) and inherently formed in integrated-circuit form since it is a compact display panel; and
- a power distributing circuit (R1-R5) connecting each of the plurality of driving devices (A1-A5) to a driving power supply source (VI1) or to a reference potential point (VI2-VI5).

Regarding Claim 26, Miyazaki discloses that a ground terminal (ground terminal is shown on the right bottom nearby VEE) of each of the integrated driving devices (A1-A5) is connected to the driving power supply source (VI1) via the power distributing circuit (R1-R5) (See Figure 2).

Regarding Claim 27, Miyazaki discloses that a ground terminal terminal (ground terminal is shown on the right bottom nearby VEE) of each of the integrated driving devices (A1-A5) is connected to the reference potential point (VI2-VI5) via the power distributing circuit (R1-R5) (See Figure 2).

Regarding Claim 33, Miyazaki discloses a capacitive load driving circuit including a configuration in which a driving power supply source (VI1-VI5 or VEE) is connected to an output terminal (V1-V5) via a driving device (A1-A5), wherein the driving power supply source (VI1-VI5 or VEE) outputs a plurality of different voltage levels in a selective manner (See Figures 3 and 11 and Col. 6, lines 38-56).

Regarding Claim 35, Miyazaki discloses a capacitive load driving circuit for driving a capacitive load (C1-C5), connected to an output terminal, by a driving device (A1-A5), comprising a resistive impedance (R1-R5) inserted in series to the output terminal (V1-V5) (See Figures 2 or 3).

Regarding Claim 38, Miyazaki discloses that a driving power supply source (VI1) connected to the output terminal (V1-V5) via the driving device (A1-A5); and a power distributing circuit (R1-R5) inserted between the driving power supply source (9) and the driving device (A1-A5) (See Figure 2).

Regarding Claim 39, Miyazaki discloses that a reference potential point (VI2-VI5) connected to the output terminal (VI-V5) via the driving device (A1-A5); and a power distributing circuit (R1-R5) inserted between the reference potential point (VI2-VI5) and the driving device (A1-A5) (See Figure 2).

Regarding Claim 40, Miyazaki discloses that a plurality of driving devices (A1-A5) for driving a plurality of capacitive loads (C1-C5), inherently formed in integrated-circuit form, wherein each of the driving devices is connected to a driving power supply source (VI1) or a reference potential point (VI2-VI5) via a power distributing circuit (R1-R5) (See Figure 2).

Claim Rejections – 35 U.S.C. 102/103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 10, 11, 19, 20, 36 and 37 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Katayama et al. (6,556,177).

Regarding Claim 2, Katayama discloses that the power distributing circuit (12 and 13) is a resistive element having an impedance whose value is inherently not small than 1/10 of the value of a resistive component of the conducting impedance of the driving device (5) since the resistors (12 and 13) must be particularly high in order to regulate the high voltage from the AC source (9) and the resistive component inside the transistors (6, 7, 8) of driving device (5) are driven with small gate current (See Col. 4, lines 10-13) and 1/10 of the value of the resistive component in the driving device is intended to be very small.

Regarding Claim 3, Katayama discloses that the power distributing circuit (12 and 13) is inherently a high-power resistor having a capability to handle power higher than the allowable power of the driving device in order to regulate the high voltage from the AC source to the transistors (6, 7, 8) of the driving device (5).

Regarding Claim 10, Katayama discloses that the power distributing circuit (12 and 13) is a resistive element having an impedance whose value is inherently not small

than 1/10 of the value of a resistive component of the conducting impedance of the driving device (5) since the resistors (12 and 13) must be particularly high in order to regulate the high voltage from the AC source (9) and the resistive component inside the transistors (6, 7, 8) of driving device (5) are driven with small gate current (See Col. 4, lines 10-13) and 1/10 of the value of the resistive component in the driving device is intended to be very small.

Regarding Claim 11, Katayama discloses that the power distributing circuit (12 and 13) is inherently a high-power resistor having a capability to handle power higher than the allowable power of the driving device in order to regulate the high voltage from the AC source to the transistors (6, 7, 8) of the driving device (5).

Regarding Claim 19, Katayama discloses that the power distributing circuit (12 & 13) is a resistive element having an impedance whose value is inherently not small than 1/10 of the value of a resistive component of the conducting impedance of the driving device (5) divided by the number of driving devices since the resistors (12 and 13) must be particularly high in order to regulate the high voltage from the AC source (9) and the resistive component inside the transistors (6, 7, 8) of driving device (5) are driven with small gate current (See Col. 4, lines 10-13) and 1/10 of the value of the resistive component in the driving device is intended to be very small.

Regarding Claim 20, Katayama discloses that the power distributing circuit (12 and 13) is inherently a high-power resistor having a capability to handle power higher than the allowable power of the driving device in order to regulate the high voltage from the AC source to the transistors (6, 7, 8) of the driving device (5).

Regarding Claims 36 and 37, Katayama discloses that the power distributing circuit (12 and 13) is a resistive element having an impedance whose value is inherently not small than 1/10 or 3/10 of the value of a resistive component of the conducting impedance of the driving device (5) since the resistors (12 and 13) must be particularly high in order to regulate the high voltage from the AC source (9) and the resistive component inside the transistors (6, 7, 8) of driving device (5) are driven with small gate current (See Col. 4, lines 10-13) and 1/10 or 3/10 of the value of the resistive component in the driving device is intended to be very small.

Alternately, it would have been to one of ordinary skill in the art to tune any appropriate resistance value in Katayama in order to attain a desired output. Besides, it is also held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).* And it is not inventive to discover the optimum or workable ranges by routine experimentation merely involves routine skill in the art. *In re Aller*, 220 F. 2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Allowable subject matter

Claims 30, 31, 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

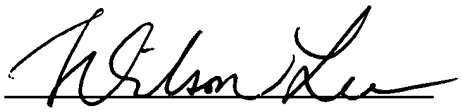
Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. DeLurio (6,376,934) discloses a voltage waveform generator comprising a

EL element with two switches and a switching power device. Buell (6,297,597) discloses a EL driver with low side current mirrors. Coghlan et al. (6,111,362) discloses a EL lamp controller with a pulse generator. Peng (5,912,535) discloses a driving circuit for an EL panel including two driving circuits.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Wilson Lee whose telephone number is (703) 306-3426. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center receptionist whose telephone number is (703) 308-0956. Papers related to Technology Center 2800 applications may be submitted to Technology Center 2800 by facsimile transmission. Any transmission not to be considered an official response must be clearly marked "DRAFT". The Technology Center Fax Center number is (703) 308-7722 or (703) 308-7724.



Wilson Lee
Patent Examiner
U.S. Patent & Trademark Office

WL
5/19/03